Maua Institute of Technology
Embedded Electronic Systems Nucleous - NSEE

Cubesat – General System and Hardware Conceptions

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ABSTRACT

This document is intended to formalize the general system and electronic hardware of the new NSEE Lab Cubesat design. The basic concepts are introduced, not as a final proposal, but as an initial idea for discussion.

The kernel design is based on three subsystems: the Application Service (APS), the quad core DPU, and the Primmary Boot Service (PBS). This last one is divided into two major systems: Communication (named “P1”), and Power Management (named “P2”).

All subsystems have a common main goal: to attend the “1U” electrical and mechanical cubesat standard specifications.

Keywords: Cubesat, Electronics, Hardware.

Summary

1. Introduction

This Cubesat conception might sound a little bit different than some usual ones, for three basic reasons.

The main reason is because there is not an attitude determination and control system (ADCS). The goal is to simplify at maximum possible level the design, for cost, power consumption, tests complexity, and time-to-market optimization.

The second reason is for the Amateur Radio Band used for ground control communication, as it will be detailed later.

Finally, the application purpose is to receive and process the Argos signals. Argos is a worldwide tracking and environmental monitoring by satellite system.

2. The Big Picture

The main idea is to have two main cpu systems, one called Quad Core DPU (Data Processing Unit), and the other called Application Service (APS).

Complementing these two cpu systems, there is another one, called Primary Boot Service (PBS), which is composed by a communication system, called P1, and a power management system, called P2.

The Quad Core DPU is responsible for data logging, general supervision, and any other kind of data processing that might be needed by APS system.

The APS system is responsible for, as it´s name says, the application computation, which is, in this particular case, to manager a Software Defined Radio (SDR) for the reception and processing of Argos (http://www.argos-system.org/) 401.650 MHz signal.

P1 system is responsible for communication, in bidirectional manner, with ground control. It uses a 144 MHz Amateur Radio Band transceiver.

P2 system is responsible for solar panels and battery charging management, and to provide power for APS and P1 systems.

The inter systems communication is done by a duplicated Controller Area Network (CAN) block.

The general system diagram is showed in fig. 1.

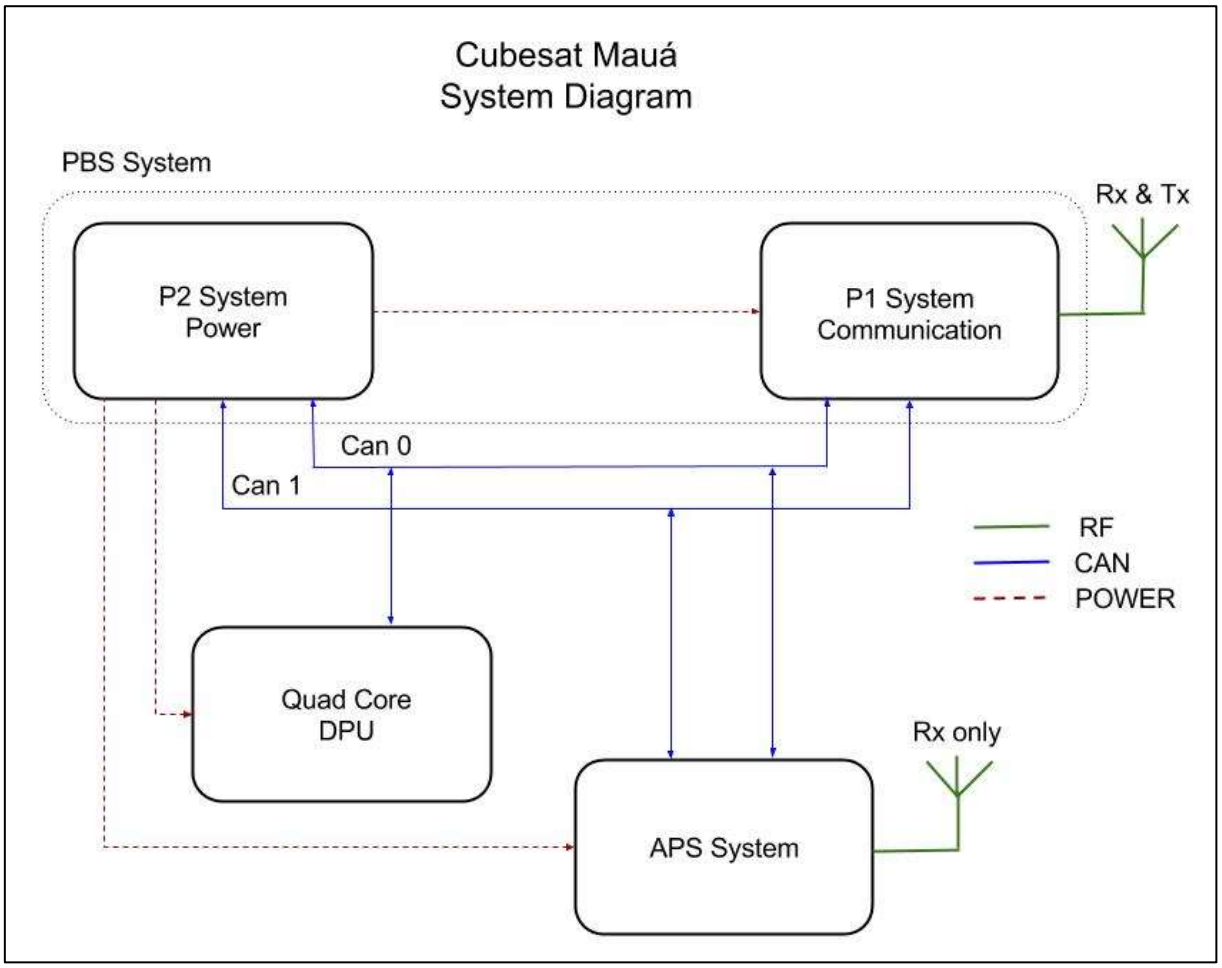


Fig. 1 - System Diagram

3. Quad Core DPU

The Quad Core DPU system is composed by four microcontrollers ARM Cortex-M4, model ATSAM4E16C.

Each microcontroller is connected to the CAN network, and the JTAG interfaces are wired in a daisy chain type.

The main board of DPU system is presented on fig. 2.

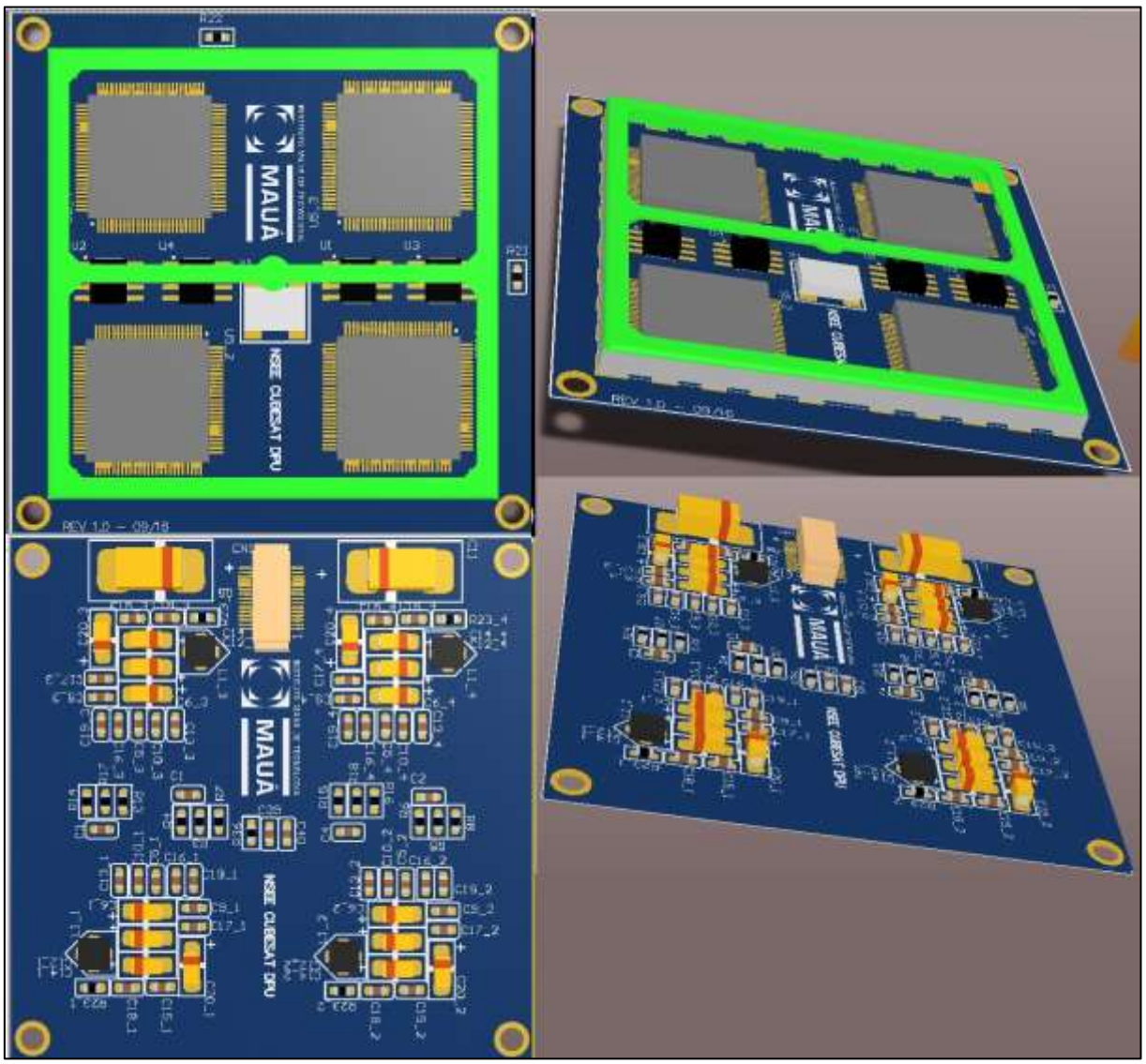


Fig. 2 - Quad Core DPU main board

4. APS

The APS block diagram is presented in fig. 3.

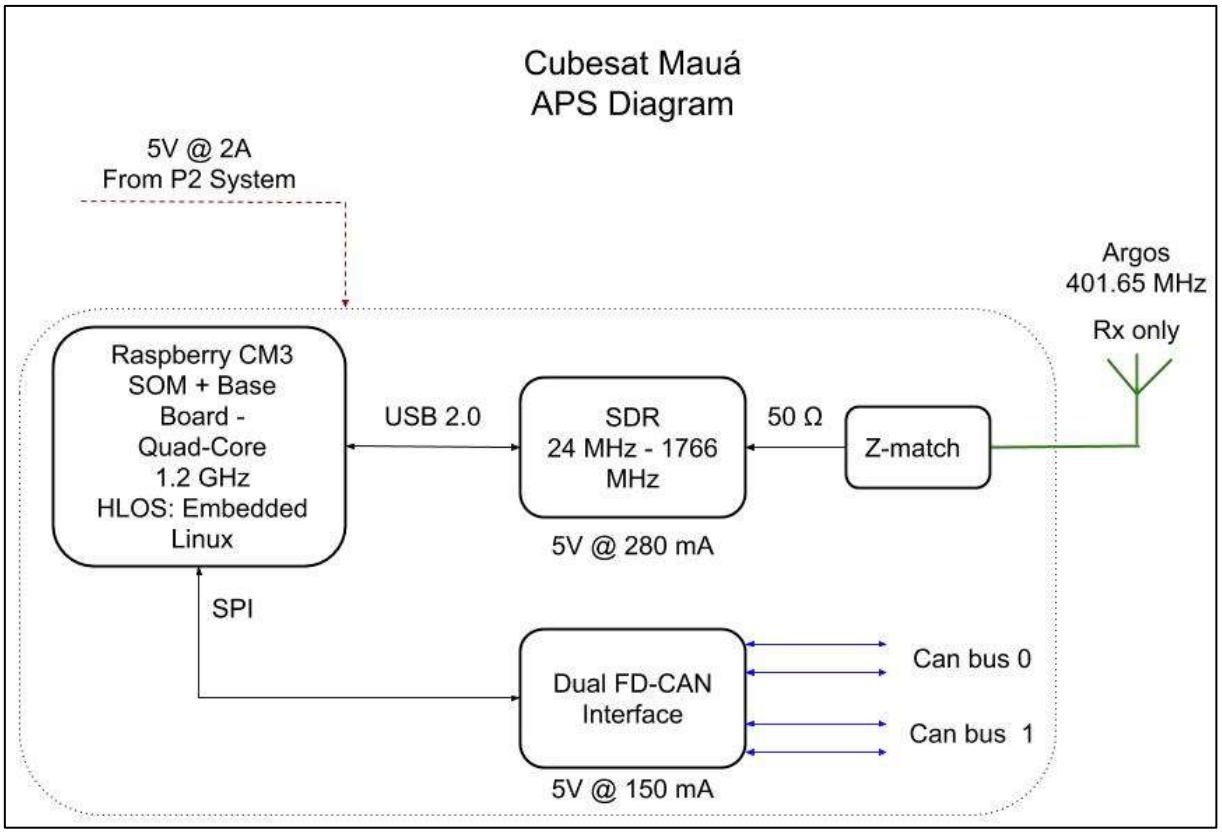


Fig. 3 - APS block diagram

There are three major blocks that have to be discussed. The first one is the CPU. The idea for CPU is to use a commercial Single Board Computer (SBC), with a powerfull processor core, at least 512 MB DDR2/3 RAM memory, and some peripherals, like USB 2.0 host, SPI, UART, among others.

The CPU has to deal with the other two major blocks: SDR and Dual CAN interface.

It´s been considered as a maximum power consumption of the whole APS system something about 5 V @ 2 A.

It´s very important to note some critical issues to choose the SBC: temperature range, and size.

It was chosen, among plenty of options, the Raspberry pi 3 CM3 module, which is a SOM (System On Module), with a DDR2 card footprint type. For that reason, a base board will be designed, for CM3 board and peripherals connections.

Fig. 4 - Raspberry Pi CM3 Module

Next, there is the APS second major block, the SDR. For the size limitation, the search for SDRs was limited to USB dongle types. The table below summarizes some reasonable options.

Cubesat - Aps SDR
Good option
Advantage
Disadvantage

Dongle Option	Core	Cpu Interface	Freq Range	Bandwidth	Size	Temperature	Antenna connector	Fob Price
AirSpy Mini	R820T2 + LPC4370	USB 2.0	24 to 1800 MHz	6 MHz	?	-10 to +40 °C	Female SMA	U$99.00
RTL-SDR V3	R820T2 + RTL2832-U	USB 2.0	24 to 1766 MHz	2.4 MHz	92 x 24.5 x 7.75 mm	?	Female SMA - 50 Ω	U$20.00
Adafruit SDR	R820T + RTL2832-U	USB 2.0	24 to 1850 MHz	?	22.24 x 23.21 x 9.9 mm	?	Female SMA	U$22.50

Fig. 5- APS SDR options

It can be seen that, for the two selected options, Airspy Mini, and RTL-SDR v3, there is a huge cost difference. AirSpy Mini seens to be more “professional” radio, but the temperature range is a problem for all of them. This is a bottom line for SDRs.

About the size issue, maybe it won´t be possible to connect a regular USB connector. Instead of that, a “connectorless” cable will have to be soldered, demanding case removing, and reassembled.

Fig. 6 - AirSpy Mini

Fig. 7 - RTL-SDR v3

Now, the third APS major block: dual CAN interface.

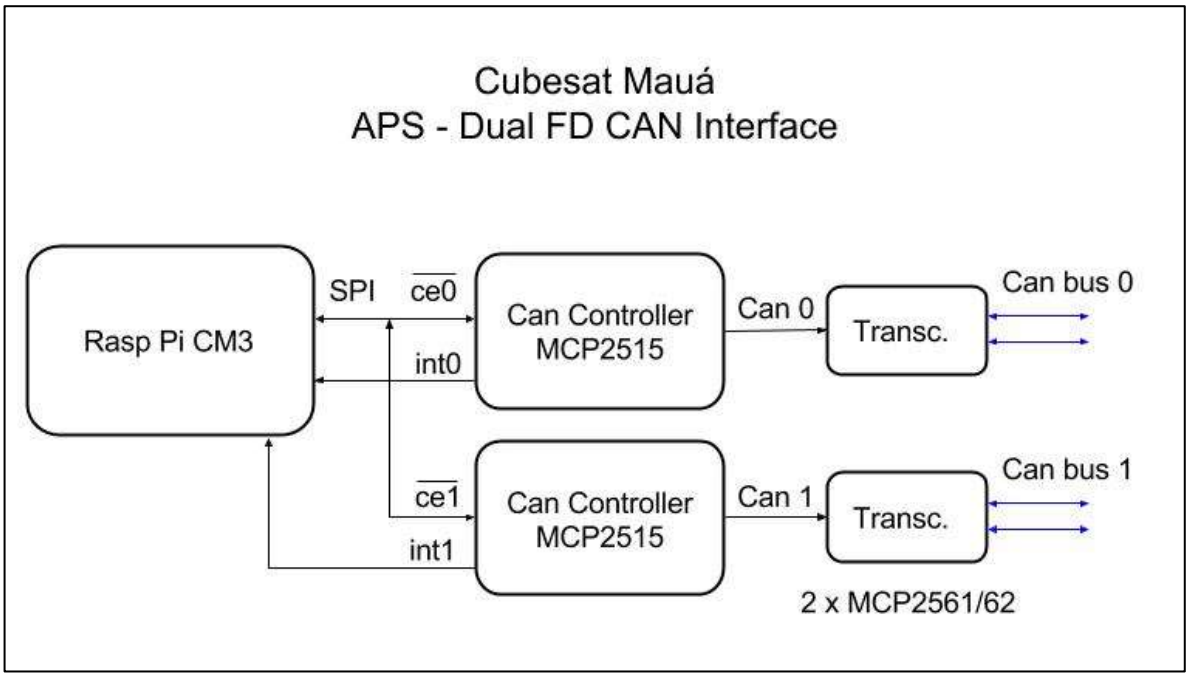
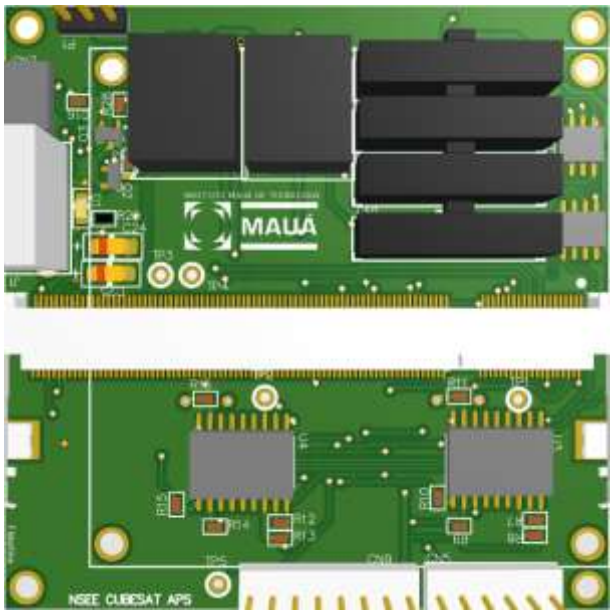
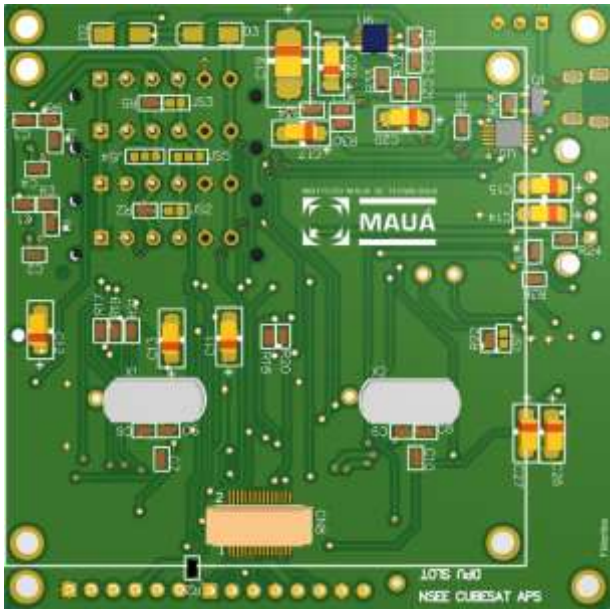


Fig. 8 - Dual CAN Interface

It can be observed that SPI interface is applied, with two chip selects, for the control of two MCP2515 external CAN controllers. Also, two gpio inputs are used in Rasp CM3, for managing interrupt outputs provided by CAN controllers (RX messages).

Below is the initial revision of board layout.

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5. P1 – Communication System

The P1 block diagram is presented in fig. 9.

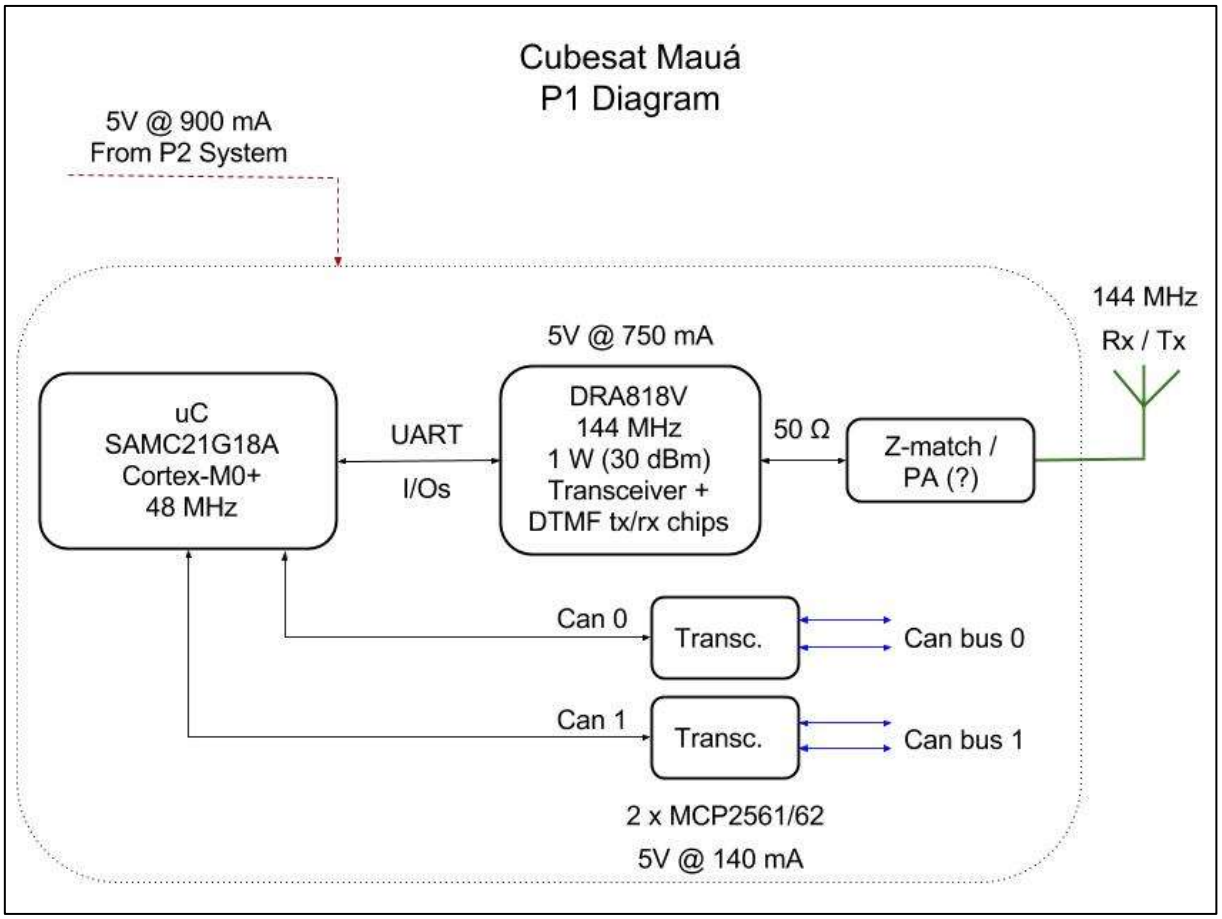
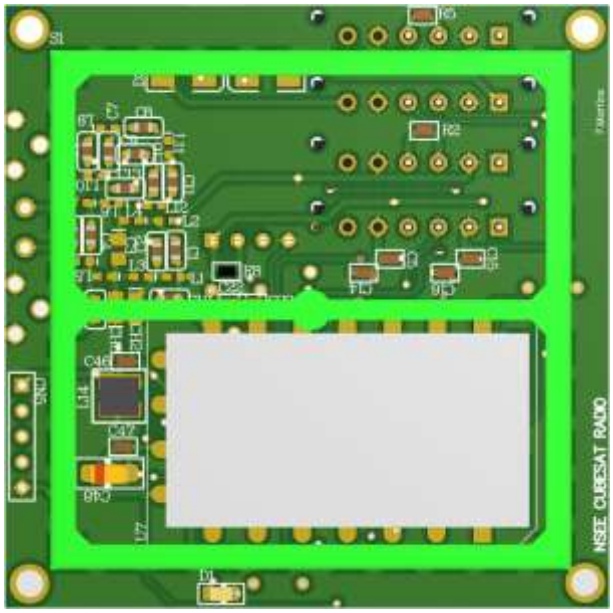


Fig. 9 - P1 Block Diagram

SAMC21G18A was chosen, primarily, for its combination of core performance, low cost, low footprint (48 pins TQFP), and two embedded CAN controllers.

P1 system, as a communication main purpose, uses a 144 MHz Amateur Radio Band (2 meters), so the RF transceiver module solution is based on an analog transceiver, DRA818V, with traditional DTMF encoder and decoder chips.

Below is the initial revision of board layout.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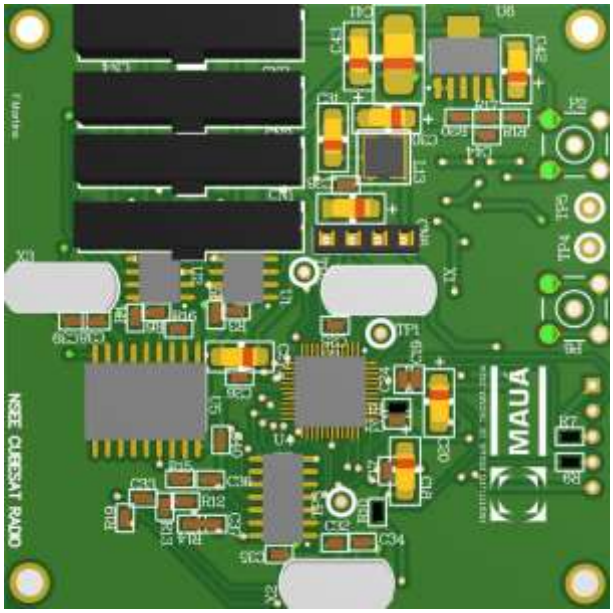
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6. P2 – Power Management System

The P2 block diagram is presented in fig. 10.

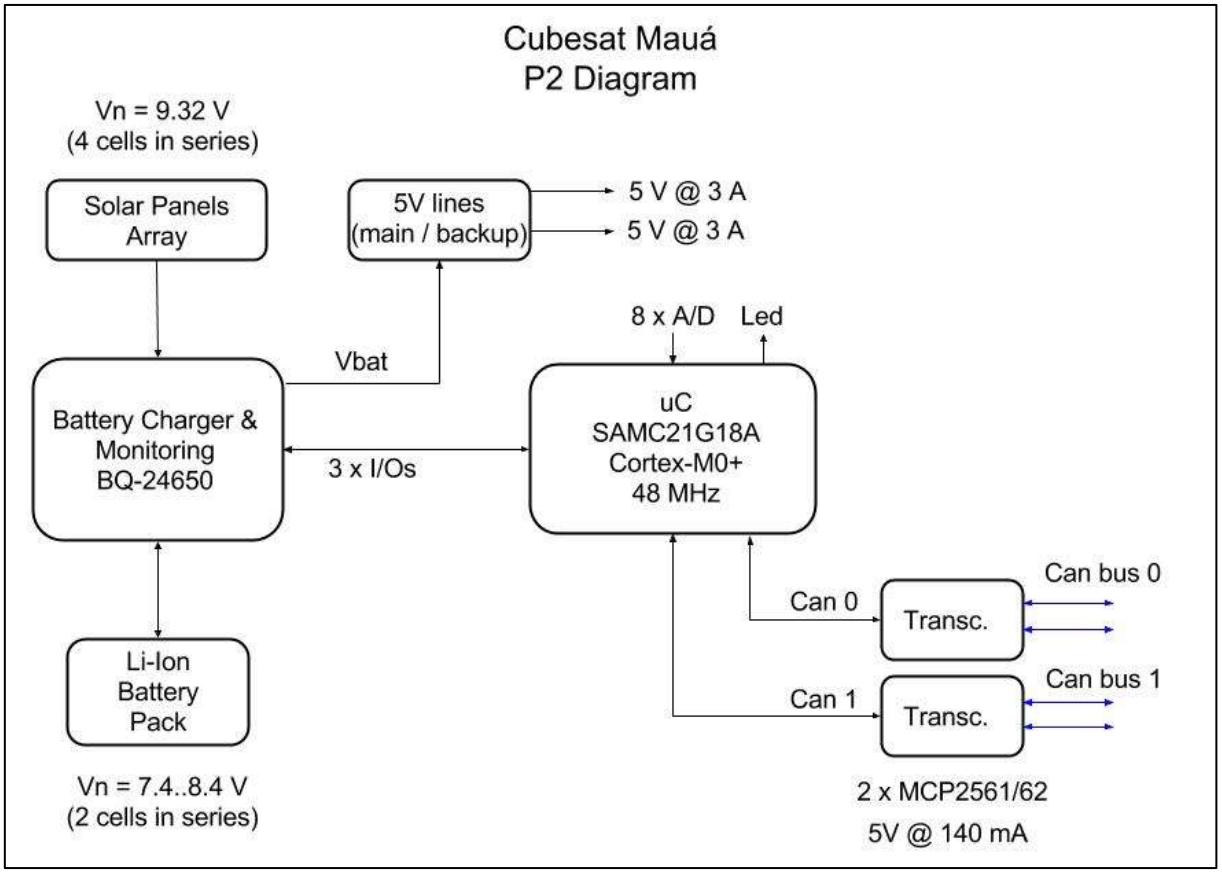
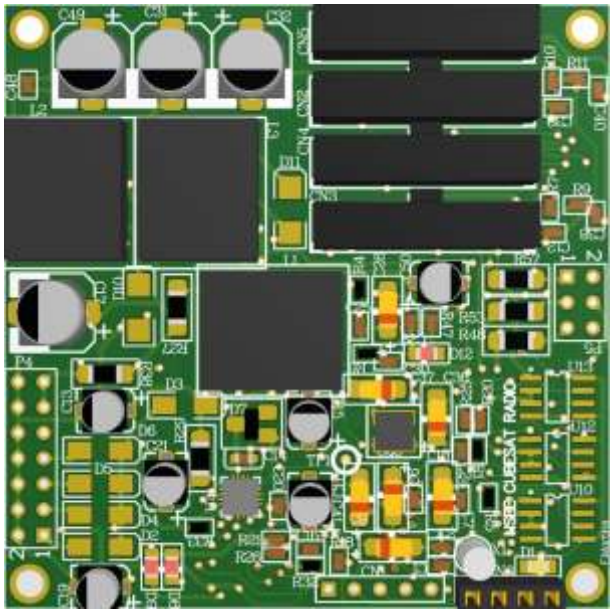


Fig. 10 - P2 Block Diagram

The principal P2 system function is the solar panels and battery management. This task is done by Texas BQ-24650 chip, a complete battery charger and monitor, applied to solar energy solutions.

It can be noted that 5V is the only power line that is delivered to DPU, P1 and APS systems. So, any cubesat module that needs 3V3 line must provide it itself.

Below is the initial revision of board layout.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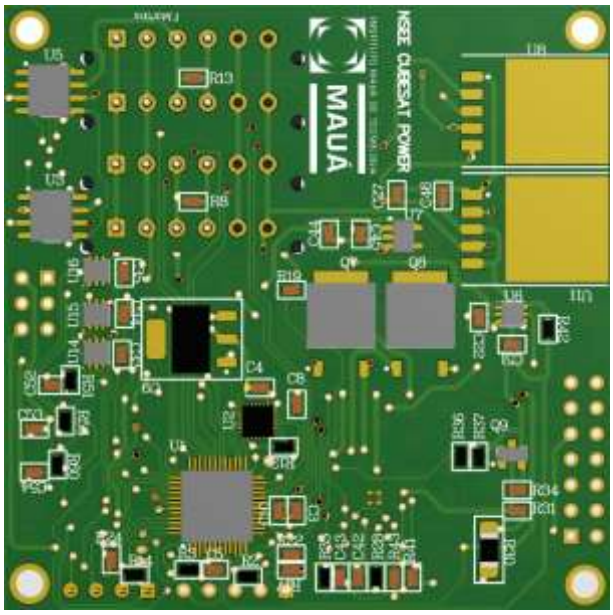
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