Electronic Design Checklist

Rev. 2.

1. During the design process, it is easy to overlook some minor detail that can result in a completely dysfunctional board with wasted time, effort, money and increased frustration as a result. I have compiled the following checklist from various sources and my own experiences. In some cases, some of the tables will be inappropriate, e.g. table 7, Software will not apply to systems that do not have a software component.

2. Use the following checklist as part of your design review. Do not release a product for prototyping, fabrication or assembly until each relevant checklist item has been verified.

3. Keep the original checklist for each version or revision so you can close the loop on the process, adding some items later if needed.

4. For each design error that occurs, add the appropriate item(s) to the list.

5. Feel free to contribute your suggestions for additions or changes so others can benefit from your experience.

6. The key to the column headings is: NA, Not Applicable; NC, Not Checked; OK, Checked and accepted.

1. Schematics

		NA	NC	OK	DATE
1	All unused inputs terminated?				
2	Race conditions checked				
3	Darlington outputs (1.2v low) driving logic inputs?				
4	Mating connectors on different assemblies checked for same pinout?				
5	Parallel busses haven't been reversed?				
6	All outside world I/O lines filtered for RFI?				
7	All outside world I/O lines protected against static discharge?				
8	Bypass cap for each IC?				
9	Voltage ratings of components checked?				
10	Ensure 3.3 volt parts are 5 volt tolerant where they interface?				
11	Verify power sequencing requirements on 5 volt and 3.3 volt rails?				
12	Each IC has predictable or controlled power-up state?				
13	File name on each sheet?				
14	Dot on each wire connection?				
15	Minimum number of characters in values?				
16	Consistent character size for readability?				
17	Schematics printed at a readable scale?				
18	All components have reference designators and values?				
19	Special PCB or parts list information entered for each component, if required?				
20	Polarized components checked?				
21	Electrolytic and tantalum capacitors checked for no reverse voltage?				
22	Power and ground pins listed for each component with hidden power pins?				
23	Check hidden power and ground connections?				
24	Title block completed for each sheet?				
25	Ground made first and breaks last for hot plugability?				
26	Pullups on all open collector outputs?				
27	Separate pullup resistors on all mode pins to allow modes to be changed if needed?				

28	Sufficient power rails for analog circuits?				
29	LM324 and LM358 outputs loaded to prevent crossover distortion?				
30	Amplifiers checked for stability?				
31	Oscillators checked for reliable startup?				
32	Consider signal rate-of-rise and fall for noise radiation?				
33	Check for input voltages applied with power off and CMOS latchup possibilities?				
34	Reset circuit design reliable, both glitch-free and consistent; tested with fast and slow power supply rise and fall time?				
35	Check RESET behavior if power cycles before the circuit is fully operational?				
36	For synchronous resets be sure the circuit can withstand unknown outputs until the clock starts?				
37	Check all resets for possible reset loops, especially for designs that are hot swap capable?				
38	Separate analog signals from noisy or digital signals?				
39	Ability to disable watchdog timer for testing and diagnostics and emulation?				
40	Sufficient capacitance on low dropout voltage regulators?				
41	Setup, hold, access times for data and address busses?				
42	Capacitance and fan out limits checked for busses?				
43	Check the data sheet fine print and appnotes for weird IC behaviors?				
44	Determine effect of losing each of multiple grounds on a connector?				
45	Automotive powered devices must withstand 60 to 100 volt surges?				
46	Check maximum power dissipation at worst-case operating temperatures?				
47	Check time delays and slew rates of OpAmps used as comparators?				
48	Check OpAmp input over-drive response for unintended output inversion?				
49	Check common mode input voltages on OpAmps?				
50	Check for voltage transients and high voltages on fet gates?				
51	Check failure modes and effects of failed power semiconductors?				
52	Estimate total worst case power supply current?				
53	Check pin numbers of all custom-generated parts?				
54	Pinout may vary between dip and various SMD packages; library parts may not match the intended package?				
55	For buses, ensure bus order matches device order?				
56	Ensure resistors are operating within their specified power range plus safety factor? Are appropriate types being used?				
57	Resistor power ratings derated for elevated ambient temperatures?				
58	Electrolytic/tantalum capacitor temperature/voltage derating sufficient for MTBF?				
59	Check for low impedance sources driving tantalum caps, which can cause premature failure?				
60	Avoid reverse base-emitter current/voltage on bipolar transistors?				
61	Check PLD pinouts each time a PLD is recompiled?				
62	Have critical signals been identified with a net name?				
63	Check that the Oscillator output of a Micro or DSP with PLL is not used for clocking other Microprocessors or DSP.				
64	Check that high speed ADCs/DACs are not receiving the conversion start signal from a DSP or Microprocessor with a PLL. (jitter)				
65	Check that a DDS (Direct Digital Synthesizer) does not get clocked by a clock, generated by a PLL inside a DSP or Microprocessor. (SFDR suffers with jittery clocks)				

2. Preferred Component Reference Designators (Ref: ANSI Y32.2-1975)

			NA	NC	OK	DATE
1	R	Resistor, fixed				
2	RN	Resistor Network				
3	RV	Resistor, Variable (Rheostat or Potentiometer)				
4	C	Capacitor; fixed or variable				
5	CN	Capacitor Network				
6	L	Inductor; Choke, Coil, Solenoid, Winding				
7	Q	Transistor, FET, SCR, TRIAC				
8	D, CR	Diode, Rectifier, Zener, varicap, LED				
9	DS	Lamp; fluorescent, glow, pilot, incandescent , LED, Display any type				
10	VR	Voltage Regulator				
11	U, IC	Integrated Circuit				
12	J	Jack (female), Connector (receptical), Socket, OR the half that is stationary				
13	P	Plug (male), Disconnecting device, OR the half that is attached to a cable/wire				
14	JP	Jumper (pins, trace, or wire)				
15	Y	Crystal				
16	M	Meter, modular subassembly, daughter board				
17	S	Switch, mechanical				
18	F	Fuse or cutout				
19	E	Ferrite; Bead, Ring				
20	AR	Amplifier; Operational, Summing,				
21	CB	Circuit breaker				
22	K	Relay				
23	DL	Delay function, line				
24	FL	Filter				
25	LS	Loud Speaker, Horn				
26	T	T Transformer , Autotransformer				
27	TB	TB Terminal Block				
28	KB	KB Keyboard				
29	BT	BT Battery				
30	Z	Z Phase changing network				

3. Parts Lists

		NA	NC	OK	DATE
1	Each component has quantity, reference designator and description				
2	List qualified part numbers for special devices				
3	Suggested and alternate manufacturer(s) listed				
4	Object/binary code and method/programmer specified for each programmable device				
5	Price and availability checked for each component				
6	Specify XTAL manufacturer and part precisely. The frequency alone is not sufficient. (may cause oscillator mailfunction during series production)				

4. PCB Design

		NA	NC	OK	DATE
1	Digital busses haven't been reversed i.e. MSB <-> LSB?				

2	Hole diameter on drawing are finished sizes, after plating?				
3	Finished hole sizes are >=10 mils larger than lead, or larger spec dictated by automatic insertion gear?				
4	Silkscreen legend text weight >=10 mils?				
5	Pads >=15 mils larger than finished hole sizes?				
6	Place thruhole components on 50 mil grid?				
7	No silkscreen legend text over vias (if vias not soldermasked) or holes?				
8	Soldermask does or does not cover vias?				
9	All legend text reads in one or two directions?				
10	Components labeled left-right, top-bottom?				
11	Company logo in silkscreen legend?				
12	Company logo in foil?				
13	Copyright notice on PCB?				
14	Date code on PCB?				
15	PCB part number and layer number on each layer in copper?				
16	Assembly part number on PCB?				
17	All polarized components point same way?				
18	Components >=0.2" from edge of PCB?				
19	Ground planes where possible?				
20	Test pad or test via on every net to allow in circuit test?				
21	For in-circuit test, no logic pins connected directly to power or ground (i.e. use pull-up resistor)?				
22	Test point on all unused outputs for use in debug?				
23	Test pads 200 mils from edge of board?				
24	Mounting holes electrically isolated or not?				
25	Mounting holes with or without islands?				
26	Proper mounting hole clearance for hardware?				
27	All polarized components checked?				
28	No acute inside angles in foil?				
29	Traces >= 20 mils from edge of PCB?				
30	PCB revision on silkscreen legend?				
31	Assembly revision blank on silkscreen legend?				
32	Serial number blank on silkscreen legend?				
33	Soldermask swell checked?				
34	Thru hole drill tolerance noted?				
35	Thru hole soldermask tolerance noted?				
36	Thru hole route tolerance noted?				
37	Thru hole silkscreen legend tolerance noted?				
38	Drill legend shows all symbols and sizes?				
39	Mounting holes matched 1:1 with mating parts?				
40	Automated netlist check?				
41	Manual netlist check?				
42	Check netlist for nodes with only one connection?				
43	All nets have meaningful names with modifiers for signal polarity, differential signals, busses?				
44	Net names case insensitive, alphanumeric, name length compatible with other tools?				
45	Beware a net named nc?				
46	Verify that nodes in a netlist with more than n connections are valid?				
47	Cad design rule check?				
48	Drill origin is a tooling hole?				
49	Checkplots sent with disk based photoplot files?				
50	NC drill and photoplot file language format noted?				
51	Tools on drill plot and nc drill file cross checked?				

52	Soldermask over bare copper noted if needed?				
53	PCB thickness, material, copper weight noted?				
54	Trace and space geometry noted?				
55	Printed drill report sent with checkplots?				
56	Printed aperture table sent with checkplots?				
57	Photoplot files checked in file viewer?				
58	Test coupon on PCB containing minimum geometry features?				
59	Trace width sufficient for current carried?				
60	Minimum component body spacing?				
61	SMD pad shapes checked?				
62	Visual references for automated assembly?				
63	Tooling holes for automated assembly?				
64	Tooling and mounting holes have internal plane clearance to avoid multilayer shorts?				
65	Sufficient clearance for high voltage traces?				
66	Component and trace keepout areas observed?				
67	High frequency circuitry precautions observed?				
68	Thermal reliefs for internal power layers?				
69	Solder paste mask openings are proper size?				
70	Blind and buried vias allowed on multilayer PCB?				
71	PCB layout panelized correctly?				
72	Panelized PCB fits test and manufacturing equipment?				
73	Breaking or cutting apart panelized PCBs after loading can stress/crack SMD parts near the break points; place parts away from stress areas?				
74	Sufficient clearance for socketed ICs?				
75	SMD component orientation arbitrary or consistent?				
76	Ensure pin 1 interpretation and orientation consistent among all connectors of a given type on the board?				
77	Clearance for IC extraction tools?				
78	Clearance for emulator adapter?				
79	Clearance for sockets for ICs during proto phase?				
80	Standoffs on power resistors or other hot components?				
81	Digital and analog signal commons joined at only one point?				
82	EMI and RFI filtering as close as possible to exit and entry points in shielded areas?				
83	Layout PCB so that any rework or repair of a component does not require removal of other components?				
84	Extra connector and IC pins accessible on prototype boards, just in case?				
85	Check all power and ground connections to ICs?				
86	Provide ground test points, accessible and sized for scope ground clip?				
87	Potentiometers should increase controlled quantity clockwise?				
88	Check hole diameters for odd components: rectangular pins, spring pins?				
89	Check the orientation of all connectors using actual connector/cable?				
90	Bypass capacitors located close to IC power pins?				
91	All silkscreen text located to be readable when the board is populated?				
92	All ICs have pin one clearly marked, visible even when chip is installed?				
93	High pin count ICs and connectors have corner pins numbered for ease of location?				
94	Silk screen tick marks for every 5th or 10th pin on high pin count ICs and connectors?				
95	Verify that all driver series terminators are located near the source?				
96	Place I/O drivers near where their signals leave the board?				
97	High frequency crystal cases flush to the PCB and grounded?				
98	Check for traces running under noisy and/or sensitive components?				

99	Check IC pin counts on layout vs schematic?				
100	No vias under metal-film resistors and similar poorly insulated parts?				
101	Check for traces, which may be susceptible to solder bridging?				
102	Maximize distances between features where possible?				
103	Check for dead-end traces?				
104	Check for PWR not shorted to GND?				
105	Ensure schematic software did / did not separate Vcc from Vdd, Vss from GND as needed?				
106	Provide multiple vias for high current and/or low impedance traces?				
107	Board outlined with overall dimensions clearly marked?				
108	Gold flash indicated?				
109	Gerber & Drill files created using the correct format?				
110	High speed buses (from DSP) must run above GND layer				
111	Check against interrupted GND layer under high speed buses or tracks				
112	Ensure to have Vdd and GND plain under a DSP to obtain best RF decoupling of supply pins.				
113	Check that track between XTAL and input pin of DSP with PLL is 5-10mm maximum.				
114	Keep track of XTAL input pin of DSPs with PLL (e.g. 218x/219x) clean from noise. Run the track "guarded" inbetween GND tracks and layer.				
115	Do not run e.g. Low-Frequency Clocks or Framing signals of Serial Ports (SPORT of DSPs) on long tracks. Keep in mind that raise/fall time is as fast as of fast buses.				
116	Check that decoupling capacitors are on silk-screen, to avoid 2 sets of through holes if GND plane is not visible.				
117	Check for multiple through holes on decoupling capacitors at high speed digital devices (DSPs).				

5. PCB Assembly

		NA	NC	OK	DATE
1	Miscellaneous parts on bill of materials and assembly notes for same: hardware, heat sinks, heat sink compound or composite insulators, IC sockets, consumables, screws, standoffs?				
2	Assembly notes for all special operations?				
3	Conformal coating required?				
4	Special static handling precautions required during assembly and test?				

6. Mechanical Drawings

		NA	NC	OK	DATE
1	Standard title block and border used				
2	No dimensions on the material				
3	Every feature must have x and y dimension, along with radius, diameter, etc.				
4	Every hole must be checked for alignment with mating hole(s) in other parts				
5	Check every hole diameter				
6	Tolerance for sheet metal feature position noted				
7	Tolerance for sheet metal hole size noted				
8	Specify material				
9	Specify finish				
10	Specify units				
11	Specify debur or brush				
12	Details for special operations				

13	File name on each sheet				
14	CAD layers shown on drawing				
15	All hardware specified and listed on parts list				
16	Screw lengths checked; extra thread required for fasteners (nut, lockwasher, washer)				
17	Hole diameters checked for each screw				
18	Tapped hole thread details indicated				

7. Software & Firmware

		NA	NC	OK	DATE
1	Each version archived for future reference				
2	Loops checked for terminating conditions				
3	Communications time-outs checked				
4	All branches tested				
5	Revision history noted for all changes				
6	CPU utilization measured				
7	Interrupt response time measured				
8	Interrupt execution time measured				
9	Naming conventions consistent and relevant to humans				
10	Adherence to coding style standards				
11	Power-up, power-down considerations				
12	Unused vectors trapped to restart or damage control routine				
13	Unused ROM space loaded with trap or restart instructions				
14	Warm and cold reset differences				
15	Nonvolatile memory corruption possibilities checked during power-up, power-down, and program-gone-wild conditions				
16	Design notes within or separate from code				
17	Check for FIFO and buffer overruns				
18	Check critical timer driver code				
19	Check for odd address usage on 16/32 bit micros, especially an odd stack pointer				
20	Use a lint utility on ‘C’ programs to find subtle problems				
21	Program's data structures contain version numbers to detect program version upgrades and translate the structures' formats				
22	Obscure code techniques and data structures adequately commented				

8. Testability (Hardware)

		NA	NC	OK	DATE
1	Test points on PCBs for critical circuits, hard to reach nets				
2	Test pads for in-circuit or bed-of-nails functional testing				
3	Test pads on a regular grid				
4	Test procedure written for each test phase				
5	Special test arrangements and connectors for testing				

9. Maintainability (Hardware)

		NA	NC	OK	DATE
1	Easy disassembly and reassembly				
2	Fuses accessible and labeled				
3	Self test mode				
4	Spare parts available				

5	Status LEDs on PCB				
6	Event logging of exceptional conditions				
7	Vibration tolerance of entire assembly and individual modules				
8	Surge current magnitude through semiconductors within rating				
9	Thermal cycling excursions internal to components and assemblies within acceptable limits				
10	Capacitors mounted below or away from heat-dissipating devices such as transformers				
11	Resistance and tolerance of entire product to static discharge via any path				

10. Protection & Safety

		NA	NC	OK	DATE
1	Fuse and circuit breaker size and characteristics				
2	Fuse sizes marked near fuse holder				
3	Room to remove fuse without damaging other components				
4	Spare fuse storage				
5	Maximum voltages				
6	Shock hazards				
7	Radiated energy warnings and shields				
8	Applicable standards checked				
9	Protection against liquids and foreign objects				

11. Documentation

		NA	NC	OK	DATE
1	End-user instructions: Unpacking, how to use, warranty, service, troubleshooting, default switch positions.				
2	Service manual: Functional description of operation, Troubleshooting procedures, parts lists, helpline info				
3	Design notes: Why were significant design decisions made the way they were. Extreme limitations				
4	Other information that may be lost if designers depart the organization				

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References

1. *"http://www.chipcenter.com/eexpert/hwallace/archive.html;$sessionid$EOKODFQAAATQXJ4Y5XCSFEQ",* Hank Wallace, Chip Center Website, 5/1/99.
2. "*Electronic Drafting & Design, 4th E*d", Nicholas M. Raskhodoff, Bishop Grafics, 1982.
3. *"Printed Circuits Handbook, 4th Ed*", Clyde F. Coombs, McGraw-Hill, 1995.
4. Seminar notes, *"Design for EMI*", Daryl Gerke, Kimmel Gerke & Assoc, Ltd, Sept' 1995.
5. Seminar notes, "*High Speed PCB & System Design*", Lee Ritchey, UC, Berkeley, July 1998.
6. "*Power Bus Decoupling on Multilayer Printed Circuit Boards*", T.H. Hubing, et al, IEEE Transactions on Electromagnetic Compatibility, Vol 37, No 2, May 1995.
7. "*Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies*", IPC-D-275, Jan 1991.

8. "*HW Product PCB Checklists*", Notes from Russell Rivin, Analog Devices, Inc, Aug, 1993.
9. Miscellaneous Personal Design Notes, Larry Hurst, Analog Devices, Inc, 1999.
10. Miscellaneous Personal Design Notes, Johannes Horvath, Analog Devices, Inc. 2002

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